Extended Flag Gadgets for Near-Term Error Detection

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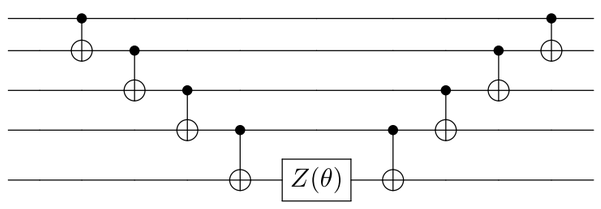
Abstract

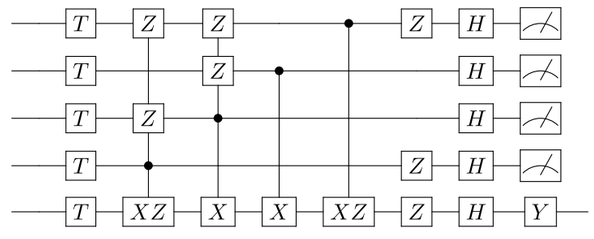
We present flag verification techniques for improving post-selected performance of near-term algorithms. We extend the definition of what constitutes a flag by creating error-detection gadgets based on known transformations of unitary operators. In some cases flags can be controlled Pauli gates. We show that such flags can improve circuit fidelities by up to a factor of 2 after post selection.

Test Circuits

ZZZZZ

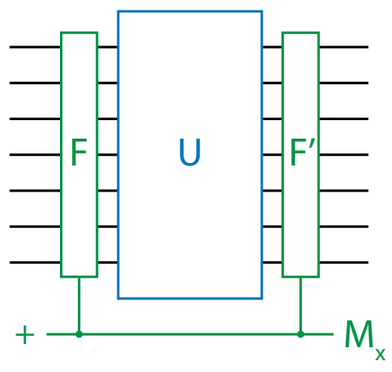


Magic State Distillation



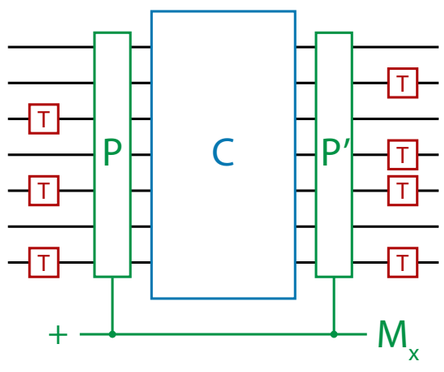
Extended Flag Gadgets

a.



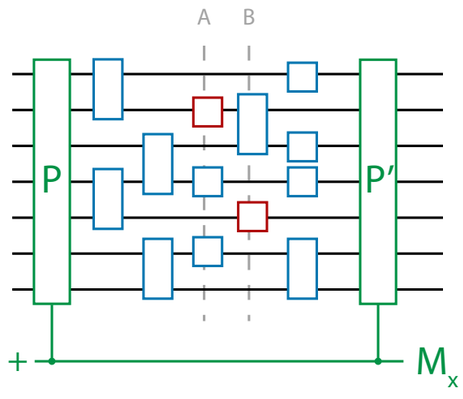
$$F' = UF^\dagger U^\dagger$$

b.



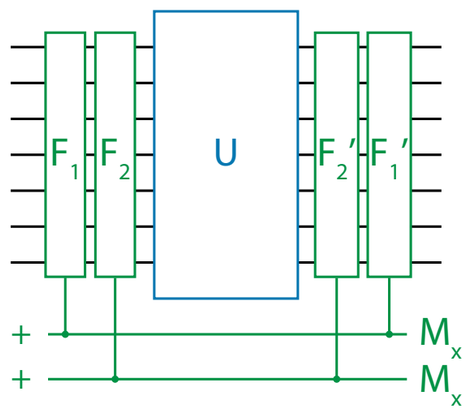
$$P' = CPC^\dagger$$

c.



$$P' = UPU^\dagger$$

d.



$$F_1' = UF_1^\dagger U^\dagger$$
$$F_2' = UF_2^\dagger U^\dagger$$

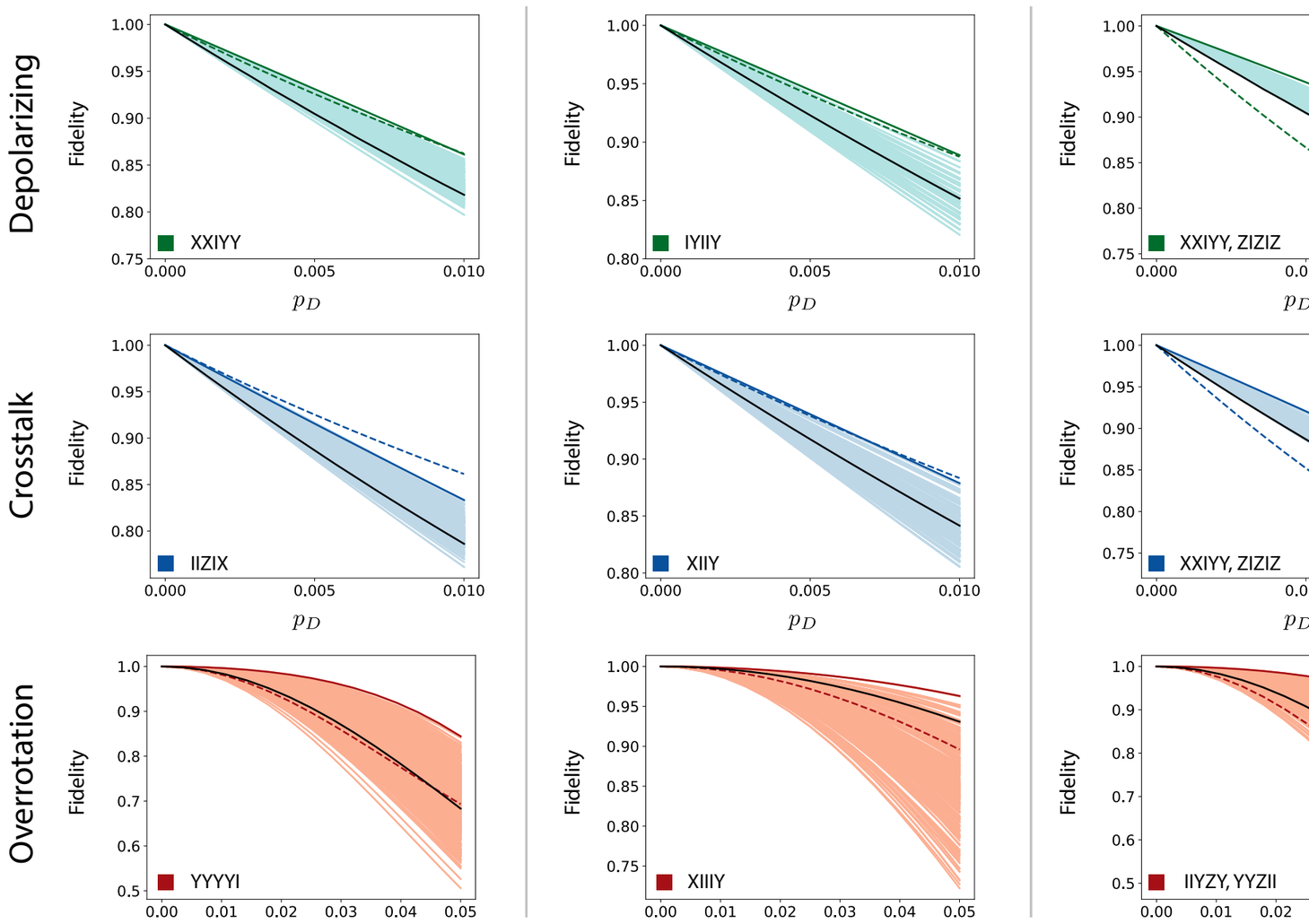
Our flag gadgets follow the same entangle-evolve-disentangle structure as the traditional flags used by Chao and Reichardt. They can detect any error which anticommutes with the F′ operator, while leaving the logic of the circuit unchanged.

Results

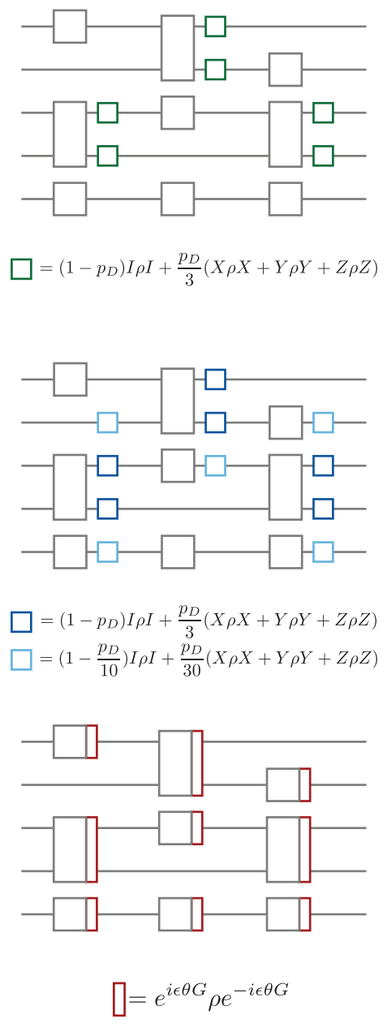
a. Distillation

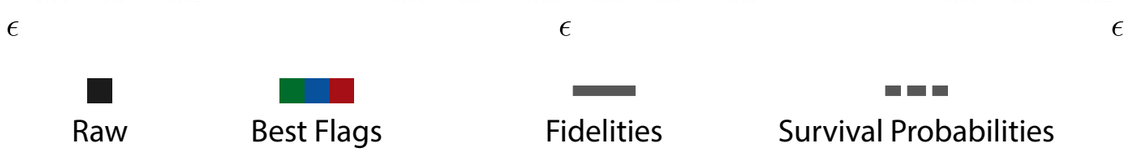
b. ZZZZZ

c. Distillation - Two Flags



Error Models





Discussion

We see that the flags perform best against denser circuits, as well as ones in which the error model is more structured. In cases where there are multiple nested flag gadgets, the inner flag can have its errors detected by the outer flag, increasing efficiency. These flags can be generated and ranked quickly on a classical computer, which makes them appealing for near-Clifford NISQ applications.

Conclusion

In this work we have presented a method for applying flag verification techniques to error detection in Clifford and near-Clifford circuits. These flags can be efficiently computed and ranked, meaning that even circuits that are outside of the range of full simulation can be protected. The flagged circuits show improvements in performance when postselected for flag success, even in cases where there are relatively few gates.

Acknowledgements

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